Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**SOURCE**

**GATE**

**.085”**

**.104”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: S = .061 X .085” G = .054 X .055”**

**Backside Potential: DRAIN**

**Mask Ref: HEX-1.5: 200V GEN 5.5 NB**

**APPROVED BY: DK DIE SIZE .085” X .104” DATE: 7/11/22**

**MFG: INT’L RECTIFIER THICKNESS .025” P/N: IRFC230NB**

**DG 10.1.2**

#### Rev B, 7/1